

Filed Via Express Mail pursuant to 37 C.F.R. 1.10

Rec No EV 096 420 885 US

On AUGUST 7, 2002

By Linda E. Hastings

LINDA E. HASTINGS

Any fee due as a result of this paper, not covered by an enclosed check, may be charged on Deposit Acct. No. 501290.

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12/9/02  
MW

Attorney Docket No.: NECW 18.159

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor: Aisushi NISHIZAWA

Serial No.: 09/751,979

Filed: December 29, 2000

Title: **MANUFACTURING METHOD OF SEMICONDUCTOR  
INTEGRATED CIRCUIT INCLUDING SIMULTANEOUS  
FORMATION OF VIA HOLE REACHING METAL WIRING  
AND CONCAVE GROOVE IN INTERLAYER FILM AND  
SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURED  
WITH THE MANUFACTURING METHOD**

Examiner: George A. Goudreau

Group Art Unit: 1763

Assistant Commissioner for Patents  
Washington, D.C. 20231

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**NOV 19 2002**  
**GROUP 1700**

**ELECTION**

SIR:

In response to the Office Action mailed on July 8, 2002, the period for responding thereto having been set to expire after August 7, 2002, Applicant hereby elects Group I, claims 1-10, and species 1, claims 4 and 7, for prosecution at this time. Applicant reserves the right to file

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continuing application(s) based on claims 5, 8, 11, and 12. Early examination on the merits is earnestly solicited.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,

  
Michael I. Markowitz  
Reg. No. 30,659

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